REMARKS

35 USC 102 – Novelty Rejections over Zaudtke

The Applicant traverses the rejections under 35 USC 102 over Omizo (US 6,654,816). In Paragraphs 3 and 21 of the Detailed Action, the examiner stated that the management functions system responds to a control signal coming from the host in a normal state based on the facts that the management functions system is able to communicate with host operating system and/or the system ROM, and would respond to a control signal from the system chip and assert a first processing signal to the peripheral I/O control device as the system chip is located between the host and the management functions system. The Applicant respectfully disagrees.

First of all, there is neither disclosure nor suggestion showing that there is indeed a control signal issued **from** the system chip **to** Zaudtke's management functions system (management processor 801) even though the management processor 801 is able to communicate with host operating system and/or the system ROM. Instead, as described in Zaudtke's col. 15, lines 56-60, the management processor 801 is used to update the system ROM 229 of the server computer 200 **by enabling the administrator 126** to execute the SETUP or configuration routine, which inherently indicates the control signal comes from the handheld device 123.

Therefore, the Applicant submits that Zaudtke's management functions system 230 or 801 fails to perform essential operations of the present control management device, i.e., the control management device asserts a first processing signal to the peripheral I/O control device in response to a control signal from the system chip in a normally operational state of the peripheral management system, and asserts a second processing signal to the peripheral I/O control device in response to an external control signal in a crash state of the peripheral management system.

35 USC 102 – Novelty Rejections over Omizo.

The Applicant traverses the rejections under 35 USC 102 over Omizo (US 6,820,119). In Paragraph 8 of the Detailed Action, the examiner cited Omizo's elements 107, 111 and 116 to be equivalent to the system chip, peripheral I/O control device and control management device, respectively. The Applicant respectfully submits the citation is improper. As described in Omizo's col. 9 line 66 through col. 10 line 4, Omizo's control management controller 116 receives recovery data through the IrDA-IF 111 and writes the recovery data directly into the BIOS-ROM 108. In other words, in a crash state, Omizo's control management device (control management controller 116) does **NOT** issue any processing signal (write recovery data) to the peripheral I/O control device (IrDA-IF 111), as the present invention does.

35 USC 103 – Nonobviousness Rejections.

The Applicant traverses the rejections under 35 USC 103 over Zaudtke et al. in view of Galfken et al. (US 5,991,841). Zaudtke et al. in view of Galfken et al. fails to disclose or suggest that the control management device asserts a first processing signal to the peripheral I/O control device in response to a control signal from the system chip in a normally operational state of the peripheral management system, and asserts a second processing signal to the peripheral I/O control device in response to an external control signal in a crash state of the peripheral management system.

The Applicant also traverses the rejections under 35 USC 103 over Zaudtke et al. in view of Mahmound (US 6,601,745). Zaudtke et al. in view of Mahmound fails to disclose or suggest that the control management device asserts a first processing signal to the peripheral I/O control device in response to a control signal from the system chip in a normally operational state of the peripheral management system, and asserts a second processing signal to the peripheral I/O control device in response to an external control signal in a crash state of the peripheral management system.

Zaudtke et al. in view of Mahmound also fails to disclose or suggest that the control management device asserts a first processing signal to the system BIOS in response to a control signal from the system chip in a normally operational state of the system BIOS, and asserts a second processing signal to the system BIOS in response to an external control signal in an idle state of the system BIOS. The examiner stated in page 6, last three lines of the Detailed Action that Mahmoud teaches a system BIOS being associated with a peripheral I/O control device to be used for initialization and configuration. Nevertheless, Zaudtke et al. in view of Mahmound still fails to disclose or suggest the remedy of the system BIOS when it becomes idle.

The Applicant further traverses the rejections under 35 USC 103 over Omizo in view of Galfken et al. Omizo in view of Galfken et al. fails to disclose or suggest that the control management device asserts a first processing signal to the peripheral I/O control device in response to a control signal from the system chip in a normally operational state of the peripheral management system, and asserts a second processing signal to the peripheral I/O control device in response to an external control signal in a crash state of the peripheral management system.

The Applicant further traverses the rejections under 35 USC 103 over Omizo. Although the examiner cited Omizo's IrDA interface to be equivalent to the present super I/O control device and the failure of a computer system to an idle state of the system chip (page 9, lines 3-13 of the Detailed Action), Omizo still fails to disclose or suggest that the control management device asserts a second processing signal **to** the super I/O control device (IrDA interface) in response to an external control signal in an idle state of the system chip. On the contrary, Omizo's control management device receives recovery data (control signal) **from** the IrDA interface.

In view of the foregoing, allowance of all pending claims is thus respectfully requested.

Respectfully submitted,

Thomas M. Hardman

/Thomas M. Hardman/

Thomas M. Hardman
Reg. No. 51,777
Attorney for Applicant

Date: October 20, 2006

MADSON & AUSTIN
Gateway Tower West
15 West South Temple, Suite 900
Salt Lake City, Utah 84101
Telephone: 801/537-1700